Advanced Power MOSFET

SSP45N20A

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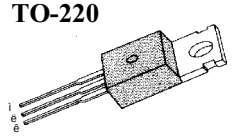
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10μA (Max.) @ V_{DS} = 200V
- Low $R_{DS(ON)}$: 0.054Ω (Typ.)

BV_{DSS} = 200 V

$R_{DS(on)}$ = 0.065Ω

I_D = 35 A

TO-220



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$EVROXWHýý0D[LPXPýý5DWLQJV

6\PER0	&KDUDFWHULVWLF	9D0XH	8QLWV
V_{DSS}	Drain-to-Source Voltage	200	V
I_D	Continuous Drain Current (T_C=25 °C)	35	A
	Continuous Drain Current (T_C=100°C)	22.2	
I_{DM}	Drain Current-Pulsed ①	140	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy ②	653	mJ
I_{AR}	Avalanche Current ①	35	A
E_{AR}	Repetitive Avalanche Energy ①	17.6	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
P_D	Total Power Dissipation (T_C=25 °C)	176	W
	Linear Derating Factor	1.41	W/°C
T_J , T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	°C
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8 " from case for 5-seconds	300	

7KHU P D0ýý5HVLVWDQFH

6\PER0	&KDUDFWHULVWLF	7\Sï	0D[ï	8QLWV
$R_{\theta JC}$	Junction-to-Case	--	0.71	°C /W
$R_{\theta CS}$	Case-to-Sink	0.5	--	
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

SAMSUNG ELECTRONICS

SSP45N20A

N-CHANNEL POWER MOSFET

(0HFWULFDOý&KDUDFWHULVWLFVý(T_C=25°C unless otherwise specified)

6\PERO	&KDUDFWHULVWLF	0LQï	7\Sï	0D[ï	8QLWV	7HVWý&RQGLWLRQ
BV_{DSS}	Drain-Source Breakdown Voltage	200	--	--	V	V_{GS}=0V ,I_D=250μA
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.21	--	V/°C	I_D=250 μA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=5V,I_D=250 μA
I_{GSS}	Gate-Source Leakage , Forward	--	--	100	nA	V_{GS}=30V
	Gate-Source Leakage , Reverse	--	--	-100		V_{GS}=-30V
I_{DSS}	Drain-to-Source Leakage Current	--	--	10	μA	V_{DS}=200V
		--	--	100		V_{DS}=160V,T_C=125 °C
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.065	Ω	V_{GS}=10V,I_D=17.5A ④
g_{fs}	Forward Transconductance	--	22.83	--	℧	V_{DS}=40V,I_D=17.5A ④
C_{iss}	Input Capacitance	--	3030	3940	pF	V_{GS}=0V,V_{DS}=25V,f =1MHz
C_{oss}	Output Capacitance	--	530	610		
C_{rss}	Reverse Transfer Capacitance	--	255	295		
$t_{d(on)}$	Turn-On Delay Time	--	22	60	ns	V_{DD}=100V,I_D=45A, R_G=5.3 Ω ④ ⑤
t_r	Rise Time	--	22	60		
$t_{d(off)}$	Turn-Off Delay Time	--	79	170		
t_f	Fall Time	--	36	80		
Q_g	Total Gate Charge	--	117	152	nC	V_{DS}=160V,V_{GS}=10V, I_D=45A ④ ⑤
Q_{gs}	Gate-Source Charge	--	25	--		
Q_{gd}	Gate-Drain(" Miller") Charge	--	48.8	--		

6RXUFHð'UDLQýý'LRGHýý5DWLQJVýýDQGýý&KDUDFWHULVWLFV

6\PERO	&KDUDFWHULVWLF	0LQï	7\Sï	0D[ï	8QLWV	7HVWý&RQGLWLRQ
I_S	Continuous Source Current	--	--	35	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	140		
V_{SD}	Diode Forward Voltage ④	--	--	1.5	V	T_J=25°C ,I_S=35A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	210	--	ns	T_J=25°C ,I_F=45A
Q_{rr}	Reverse Recovery Charge	--	1.67	--	μC	di_F/dt=100A/μs ④

1RWHVýâ

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

② L=0.8mH, I_{AS}=35A, V_{DD}=50V, R_G=27Ω , Starting T_J=25°C

③ I_{SD} ≤45A, di/dt ≤370A/μs, V_{DD}≤ BV_{DSS} , Starting T_J=25 °C

④ Pulse Test : Pulse Width = 250μs, Duty Cycle≤ 2%

⑤ Essentially Independent of Operating Temperature

Fig 7. Breakdown Voltage vs. Temp

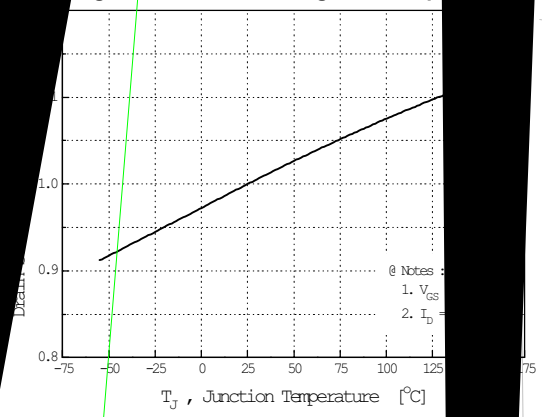

Fig 8. On-Resistance vs. Tempera

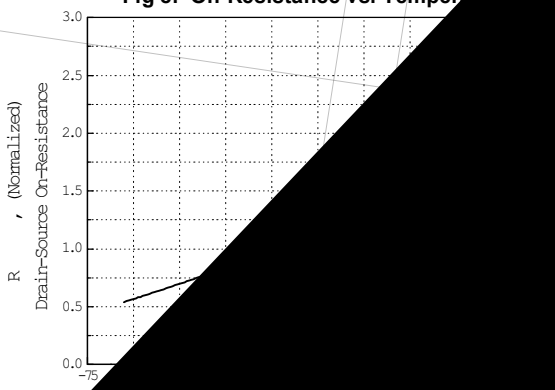

Fig 9. Max. Safe Operating Area

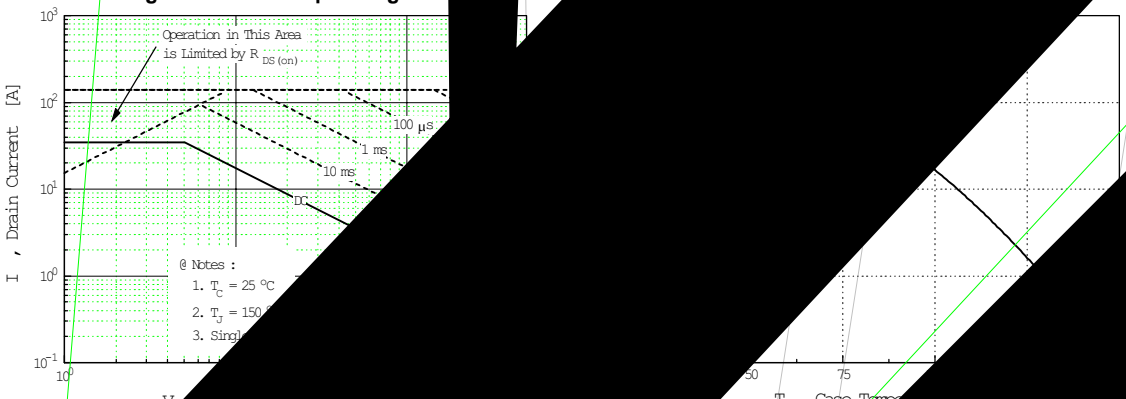

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Fig 12. Gate Charge Test Circuit & Waveform

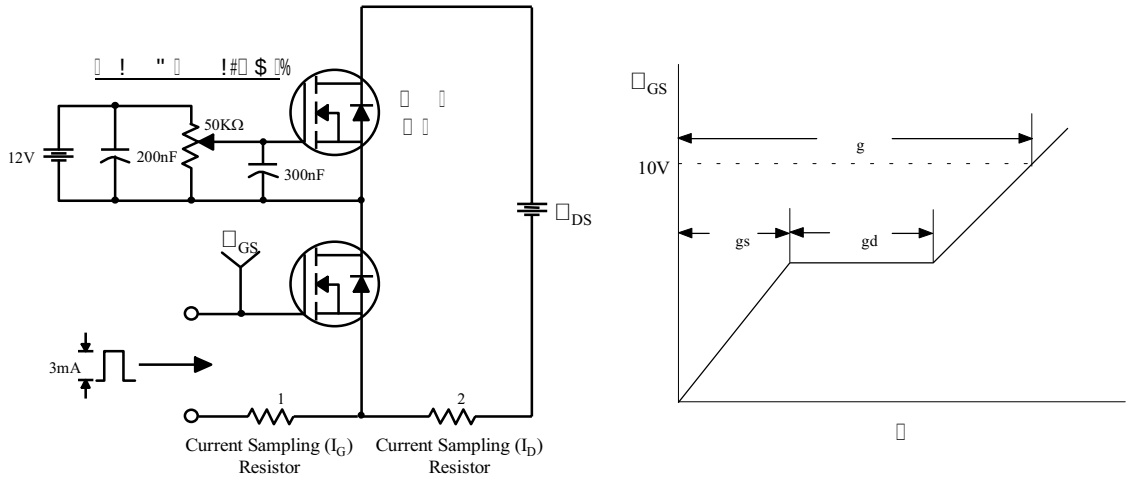

Fig 13. Resistive Switching Test Circuit & Waveforms

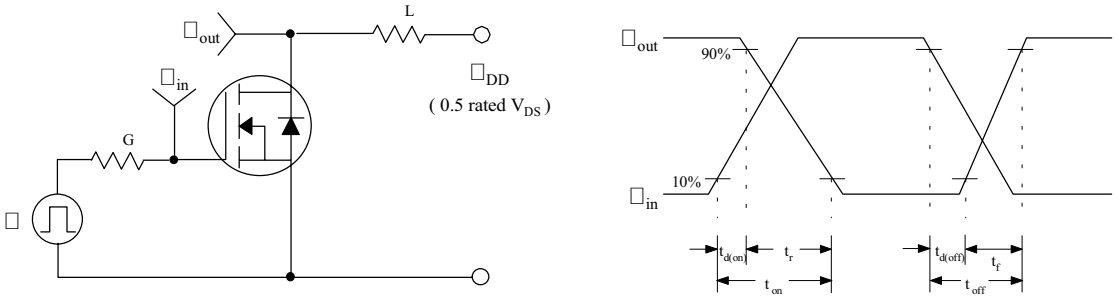

Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

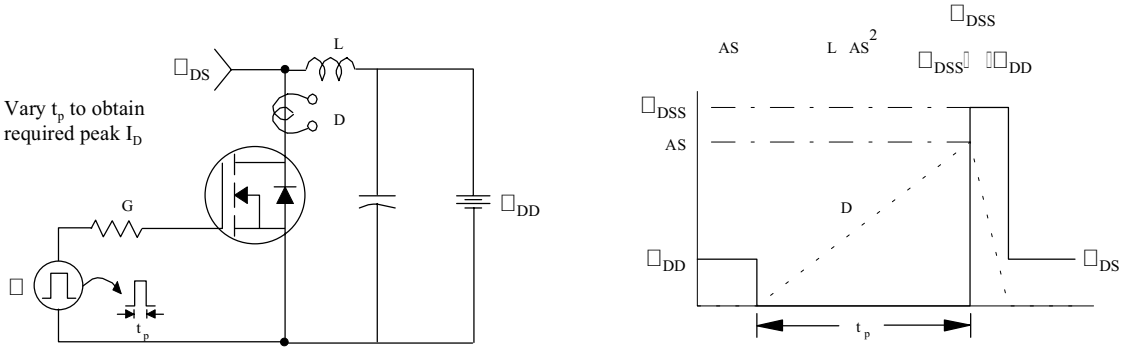

Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms